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IN THE CLAIMS

This listing of claims replaces all prior versions and listings of claims in the above-referenced application.

1. (Previously Amended) A method for manufacturing a p-type III-V nitride compound semiconductor comprising:

growing in a chamber a III-V nitride compound semiconductor layer at a first temperature while introducing acceptor impurities into said layer to form an acceptor-doped layer, said chamber containing one or more gases providing hydrogen such that said hydrogen passivates at least some of said acceptor impurities;

cooling said acceptor-doped layer to a second temperature significantly lower than said first temperature during a cool-down process;

preventing additional hydrogen from diffusing into said acceptor-doped layer substantially during the cool-down process;

causing said acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3x10^{15}cm^{-3}$ and $1x10^{18}cm^{-3}$, after said cool-down process; and

after said cooling, heating said p-type layer to a third temperature greater than the second temperature and less than 625°C to remove hydrogen from said p-type layer thereby increasing said hole density and lowering the resistivity of said p-type layer.

2. (Canceled).

3. (Previously Amended) The method of Claim 1 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises preventing gases containing hydrogen from entering said chamber during said cool-down process and removing hydrogen in said chamber during said cool-down process.

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4. (Previously Amended) The method of Claim 1 wherein said preventing

additional hydrogen from diffusing into said acceptor-doped layer comprises forming an n-type semiconductor layer cap over said acceptor-doped layer prior to said cool-down process.

5. (Original) The method of Claim 1 wherein said causing said acceptor-doped layer to be a p-type layer prior to said annealing comprises treating a surface of said acceptor-doped layer to increase said hole density at said surface to be greater than $3x10^{15}cm^{-3}$.

6. (Original) The method of Claim 5 wherein said treating said surface comprises chemically etching said surface.

7. (Original) The method of Claim 5 wherein said treating said surface comprises plasma etching said surface.

8. (Original) The method of Claim 5 wherein said treating said surface comprises plasma cleaning said surface.

9. (Original) The method of Claim 5 wherein said treating said surface comprises chemically cleaning said surface.

10. (Original) The method of Claim 9 wherein said chemically cleaning said surface comprises cleaning said surface in a solution of at least one of KOH, NaOH, and NH_40H.

11. (Original) The method of Claim 5 wherein said treating said surface comprises ultrasonically cleaning said surface.

12. (Original) The method of Claim 5 wherein said treating said surface comprises irradiating said surface with an electron-beam.

13. (Original) The method of Claim 5 wherein said treating said surface comprises exposing said surface to electromagnetic radiation.

14. (Original) The method of Claim 1 wherein said growing an acceptor-doped layer results in acceptor impurities in said acceptor-doped layer having greater than 90% passivation prior to said cool-down process.

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15. (Original) The method of Claim 1 wherein, after said cool-down process, said hole density is greater than $3x10^{16}cm^{-3}$.

16. (Original) The method of Claim 1 wherein said introducing acceptor impurities comprises doping said semiconductor layer to have a density of acceptor impurities greater than $5x10^{18}cm^{-3}$.

17. (Original) The method of Claim 1 wherein said annealing is carried out at a temperature in the range of 100-625°C.

18. (Original) The method of Claim 1 wherein said annealing is carried out at a temperature below 400°C.

19. (Original) The method of Claim 1 wherein said growing in a chamber an acceptor-doped layer is performed in a chamber different from a chamber in which said p-type layer is annealed.

20. (Original) The method of Claim 1 wherein said annealing is carried out after said cool-down process prior to any further processing of said p-type layer.

21. (Original) The method of Claim 1 wherein said growing in a chamber an acceptor-doped layer further comprises growing a III-V nitride compound n-doped semiconductor layer to form a light emitting diode.

22. (Original) The method of Claim 21 wherein said acceptor-doped layer is grown subsequent to said n-doped semiconductor layer.

23. (Original) The method of Claim 1 further comprising growing additional one or more III-V nitride compound acceptor-doped layers and causing said additional one or more acceptor-doped layers to be p-type prior to said annealing.

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24. (Original) The method of Claim 1 wherein said annealing is carried out solely to remove said hydrogen from said p-type layer.

25. (Original) The method of Claim 1 wherein said annealing is carried out to

remove said hydrogen from said p-type layer as well as to anneal or alloy a p-type ohmic contact.

26. (Original) The method of Claim 1 wherein said growing said acceptor-doped layer comprises growing a group III-V compound semiconductor including gallium and nitrogen.

27. (Original) The method of Claim 1 wherein said acceptor impurities comprise magnesium.

28. (Original) The method of Claim 1 wherein said annealing is carried out in a gas environment containing N_2.

29. (Original) The method of Claim 1 wherein the resistivity of said p-type layer prior to said annealing is less than 5000 ohm-cm.

30. (Original) The method of Claim 1 wherein the resistivity of said p-type layer prior to said annealing is less than 30 ohm-cm.

31. (Previously Amended) A method for manufacturing a p-type III-V nitride compound semiconductor comprising:

growing in a chamber a III-V nitride compound semiconductor layer at a first temperature while introducing acceptor impurities into said layer to form an acceptor-doped layer, said chamber containing one or more gases providing hydrogen such that said hydrogen passivates at least some of said acceptor impurities;

cooling said acceptor-doped layer to a second temperature significantly lower than said first temperature during a cool-down process, thereby causing said acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3x10^{15}cm^{-3}$ and $1x10^{18}cm^{-3}$, after said cool-down process; and

after said cooling, heating said p-type layer to a third temperature greater than the second temperature and less than 625°C to remove hydrogen from said p-type layer thereby

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increasing said hole density and lowering the resistivity of said p-type layer.

32. (Previously Added) The method of Claim 31 further comprising substantially preventing additional hydrogen from diffusing into said acceptor-doped layer during said cooling process.

33. (Previously Amended) The method of Claim 32 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises preventing gases containing hydrogen from entering said chamber during said cool-down process and removing hydrogen in said chamber during said cool-down process.

34. (Previously Amended) The method of Claim 32 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises forming an n-type semiconductor layer cap over said acceptor-doped layer prior to said cool-down process.

35. (Previously Added) The method of Claim 31 further comprising treating a surface of said acceptor-doped layer to increase said hole density at said surface to be greater than $3x10^{15}cm^{-3}$.

36. (Previously Added) The method of Claim 35 wherein said treating said surface comprises chemically etching said surface.

37. (Previously Added) The method of Claim 35 wherein said treating said surface comprises plasma etching said surface.

38. (Previously Added) The method of Claim 35 wherein said treating said surface comprises plasma cleaning said surface.

39. (Previously Added) The method of Claim 35 wherein said treating said surface comprises chemically cleaning said surface.

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40. (Previously Added) The method of Claim 39 wherein said chemically cleaning said surface comprises cleaning said surface in a solution of at least one of KOH, NaOH, and NH_4OH.

41. (Previously Added) The method of Claim 35 wherein said treating said surface comprises ultrasonically cleaning said surface.

42. (Previously Added) The method of Claim 35 wherein said treating said surface comprises irradiating said surface with an electron-beam.

43. (Previously Added) The method of Claim 35 wherein said treating said surface comprises exposing said surface to electromagnetic radiation.

44. (Previously Added) The method of Claim 31 wherein said growing an acceptor-doped layer results in acceptor impurities in said acceptor-doped layer having greater than 90% passivation prior to said cool-down process.

45. (Previously Added) The method of Claim 31 wherein, after said cool-down process, said hole density is greater than $3x10^{16}cm^{-3}$.

46. (Previously Added) The method of Claim 31 wherein said introducing acceptor impurities comprises doping said semiconductor layer to have a density of acceptor impurities greater than $5x10^{18}cm^{-3}$.

47. (Previously Added) The method of Claim 31 wherein said annealing is carried out at a temperature in the range of 100-625°C.

48. (Previously Added) The method of Claim 31 wherein said annealing is carried out at a temperature below 400°C.

49. (Previously Added) The method of Claim 31 wherein said growing in a chamber an acceptor-doped layer is performed in a chamber different from a chamber in which said p-type layer is annealed.

50. (Previously Added) The method of Claim 31 wherein said annealing is carried out after said cool-down process prior to any further processing of said p-type layer.

51. (Previously Added) The method of Claim 31 wherein said growing in a chamber an acceptor-doped layer further comprises growing a III-V nitride compound n-

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doped semiconductor layer to form a light emitting diode.

52. (Previously Added) The method of Claim 51 wherein said acceptor-doped layer is grown subsequent to said n-doped semiconductor layer.

53. (Previously Added) The method of Claim 31 further comprising growing additional one or more III-V nitride compound acceptor-doped layers and causing said additional one or more acceptor-doped layers to be p-type prior to said annealing.

54. (Previously Added) The method of Claim 31 wherein said annealing is carried out solely to remove said hydrogen from said p-type layer.

55. (Previously Added) The method of Claim 31 wherein said annealing is carried out to remove said hydrogen from said p-type layer as well as to anneal or alloy a p-type ohmic contact.

56. (Previously Added) The method of Claim 31 wherein said growing said acceptor-doped layer comprises growing a group III-V compound semiconductor including gallium and nitrogen.

57. (Previously Added) The method of Claim 31 wherein said acceptor impurities comprise magnesium.

58. (Previously Added) The method of Claim 31 wherein said annealing is carried out in a gas environment containing N_2.

59. (Previously Added) The method of Claim 31 wherein the resistivity of said p-type layer prior to said annealing is less than 5000 ohm-cm.

60. (Previously Added) The method of Claim 31 wherein the resistivity of said p-type layer prior to said annealing is less than 30 ohm-cm.

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